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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,696	03/22/2004	Hyung-Rok Oh	8836-231 (ID13030-US)	8731

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WOODBURY, NY 11797

EXAMINER

TRAN, MAI HUONG C

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/805,696

Applicant(s)

OH ET AL.

Examiner

Mai-Huong Tran

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6-7 and 17 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,750,469 to Ichihara et al. (hereinafter Ichihara).

Regarding to claim 1, Ichihara discloses a phase random access memory having a memory cell array arranged with a plurality of component areas, each of the component areas comprising a first conductive line (col. 11, lines 66-67) extending in a first direction; a plurality of second conductive lines (col. 11, lines 53-55) extending in a second direction; a phase-changeable film 16 electrically connected to the first conductive line 15; a first semiconductor region 13 electrically connected to the phase-changeable film and defined within a first active region; and a second semiconductor region 14 defined within a second active region and separated from the first semiconductor region 13 (col. 11, lines 25-67, and figs. 1B and 2).

Regarding to claim 6, Ichihara discloses the phase random access memory wherein the first conductive line is a bitline 34 and wherein each of the plurality of second conductive lines is a wordline 32 (col. 11, lines 10-14).

Regarding to claim 7, Ichihara discloses a phase random access memory comprising a bitline 15; a plurality of access transistors 30, each access transistor including a drain region; and a phase-changeable film 16 shared by the plurality access transistors 30 (col. 11, lines 4-67, and figs. 1B and 2).

Regarding to claim 17, Ichihara discloses a phase random access memory having a memory cell array arranged with a plurality of component areas, each of the component areas comprising a first conductive line (col. 11, lines 66-67) extending in a first direction; a plurality of second conductive lines (col. 11, lines 53-55) extending in a second direction; a plurality of phase-changeable films 16 electrically connected to the first conductive line 15; and a semiconductor region 13/14 electrically connected to the plurality of phase-changeable films, wherein at least one phase-changeable film of the plurality of phase changeable films is electrically connected to an adjacent semiconductor region of an adjacent component area (col. 11, lines 25-67, and figs. 1B and 2).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-5, 8-16, and 18-20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,750,469 to Ichihara et.al. in view of the remark.

Regarding to claims 4 and 5, Ichihara discloses the claimed invention except for the phase random access memory wherein each of the component areas further comprises a plurality of third conductive lines extending in the second direction, wherein the plurality of third conductive lines are ground lines. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of third conductive lines that are ground lines.

Regarding to claim 8, Ichihara discloses the phase random access memory wherein the phase-changeable film is connected to the bitline through a first electrode and connected to each respective drain region through at least one of a plurality of second electrodes (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 9, Ichihara discloses the phase random access memory wherein the plurality of access transistors share the first electrode (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 10, Ichihara discloses the phase random access memory wherein a source region of each access transistors is connected to a respective ground line (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 11, Ichihara discloses the phase random access memory wherein the drain and source regions of each access transistor are defined within an active region (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 12, Ichihara discloses the phase random access memory wherein the active region is divided into a plurality of regions isolated from each other (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 13, Ichihara discloses the phase random access memory wherein a source region of each access transistor is commonly connected to a ground line (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 14, Ichihara discloses the phase random access memory wherein the ground line is shared by the source region of each access transistor (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 15, Ichihara discloses the phase random access memory wherein the plurality of access transistors share a source region (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 16, Ichihara discloses the phase random access memory wherein the phase-changeable film is connected to the bitline through a bitline contact shared by the drain region of each access transistor (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 18, Ichihara discloses the phase random access memory further comprising a plurality of bitline contacts through which the plurality of phase changeable films are connected to the semiconductor region, wherein at least one bitline contact of the plurality of bitline contacts connects the at least one phase-changeable film to the adjacent semiconductor region (col. 11, lines 4-65, figs. 1B and 2).

Regarding to claim 19, Ichihara discloses the phase random access memory further comprising a third conductive line, wherein at least one of third conductive line and the plurality of second conductive lines are twisted (col. 11, lines 4-65, figs. 1B and 2).


Regarding to claim 20, Ichihara discloses the phase random access memory wherein the first conductive line is a bitline, each of the plurality of second conductive lines is a wordline, and the third conductive line is a ground line (col. 11, lines 4-65, figs. 1B and 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Mai-Huong Tran
Examiner
Art Unit 2818